

CLAIMS

I claim:

1. A hardware unit within a digital signal processor (DSP), comprising:

5           four polarity circuits, each configured to receive an input value and calculate a negative of the input value;

          four sets of multiplexers, each set comprising two multiplexers, wherein each of the  
10       multiplexers in each set receives a corresponding input signal and a corresponding output signal from one of the four polarity circuits;

          a code register coupled to each of the multiplexers, wherein code bits within the code  
15       register determine which input the multiplexers select;

          four first arithmetic circuits selectively coupled to receive signals from the multiplexers;

          two second arithmetic circuits selectively  
20       coupled to receive signals from the multiplexers; and

          two second multiplexers, each configured to receive an output signal from one of the second arithmetic circuits and an output signal from the  
25       first arithmetic circuits.

2. The hardware unit of Claim 1, further comprising a bus coupled between the multiplexers and the first arithmetic circuits.

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3. The hardware unit of Claim 1, wherein the code register comprises in-phase and quadrature code

registers.

4. The hardware unit of Claim 1, wherein the  
input signal comprises in-phase and quadrature data bit  
5 signals.

5. The hardware unit of Claim 1, wherein the  
hardware unit performs complex scrambling and complex  
correlation functions.  
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6. The hardware unit of Claim 5, wherein the  
hardware unit further performs spreading operations.

7. The hardware unit of Claim 5, wherein the  
15 hardware unit supports IS-95 and WCDMA.

8. The hardware unit of Claim 7, wherein the  
hardware unit further supports cdma2000.

20 9. The hardware unit of Claim 1, further  
comprising a second hardware unit comprising:  
a first multiplexer configured to receive  
data bits;  
a set of 2-to-1 multiplexers configured to  
25 receive the data bits and the output of the first  
multiplexer; and  
a set of logic gates configured to receive  
code sequence bits and the output of the 2-to-1  
multiplexers.

30 10. The hardware unit of Claim 9, wherein the  
logic gates are exclusive-OR gates.

11. The hardware unit of Claim 9, wherein the second hardware unit performs spreading operations for IS-95.

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12. The hardware unit of Claim 9, wherein the first multiplexer is a 4-bit 3-to-1 multiplexer.

13. The hardware unit of Claim 9, wherein the set  
10 is equal 16.

14. The hardware unit of Claim 4, wherein the input signal is in a 4-bit format.

15 15. The hardware unit of claim 4, wherein the input signal is in a 8-bit format.

16. The hardware unit of Claim 1, wherein the most significant bits of the code register determine  
20 which input the multiplexers select.

17. The hardware unit of Claim 1, wherein the second arithmetic circuits are configured to receive concatenated signals from the four sets of  
25 multiplexers.

18. The hardware unit of Claim 1, wherein the four sets of multiplexers are 2-to-1 multiplexers.

19. The hardware unit of Claim 1, further  
30 comprising four second multiplexers, each configured to receive signals from the multiplexers and the first

arithmetic circuits and coupled to one of the second arithmetic circuits.

20. The hardware unit of Claim 19, further  
5 comprising two third arithmetic circuits configured to receive the output signals from the second arithmetic circuits and two registers configured to receive the output signals from the third arithmetic circuits, wherein each register is coupled to an input of one of  
10 the third arithmetic circuits.

21. A hardware unit within a CDMA unit within a digital signal processor (DSP), the hardware unit  
comprising:

15 means for calculating the negative of an input signal;  
2-to-1 multiplexers coupled to the means for calculating, wherein each of the multiplexers selects either the input signal or the negative of  
20 the input signal;  
a code register coupled to each of the multiplexers, wherein code bits within the code register determine which input the multiplexers select;  
25 first arithmetic circuits coupled to the output of the multiplexers to add or subtract inputs to the arithmetic circuits;  
second arithmetic circuits coupled to at least the 2-to-1 multiplexers; and  
30 two multi-bit 2-to-1 multiplexers coupled to the second arithmetic circuits, wherein the multi-bit 2-to-1 multiplexers select signals for use by

the DSP.